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DESIGN AND VALIDATION CHALLENGES IN MODERN FPGA BASED SOC SYSTEMS

Ashvini Byri[1], Phanindra Kumar Kankanampati[2], Abhishek Tangudu[3], Om Goel[4], Ojaswin Tharan[5] & Prof.(Dr.) Arpit Jain[6]

[1]Scholar, University of Southern California, Parel, Mumbai 400012, India

[2]Scholar, Binghamton University, Glenmallen Ln, Richmond, Tx 77407

[3]Scholar, Campbellsville University, USA

[4]Independent Researcher, Abes Engineering College Ghaziabad, India

[5]Independent Researcher, Knowledgeum Academy, Karnataka, India

[6]Independent Researcher, KL University, Vijaywada, Andhra Pradesh, India

ABSTRACT

The rapid evolution of Field-Programmable Gate Array (FPGA)-based System-on-Chip (SoC) systems has transformed the landscape of digital design, enabling unprecedented flexibility and performance. However, this advancement introduces significant design and validation challenges. This paper addresses the complexities associated with integrating diverse components within FPGA-based SoC systems, focusing on issues such as design methodology, tool compatibility, and system integration. The intricate interplay between hardware and software necessitates a robust design flow that can accommodate rapid prototyping and iterative refinement. Moreover, validation processes must adapt to ensure reliable functionality, encompassing both hardware verification and software validation. Key challenges include the management of timing constraints, debugging in a high-density environment, and ensuring the overall system integrity. The paper also explores emerging solutions, including high-level synthesis and automated validation frameworks, which aim to streamline the design process while enhancing verification accuracy. By identifying and addressing these challenges, this study provides insights into best practices and methodologies that can facilitate the successful implementation of modern FPGA-based SoC systems. The findings underscore the importance of a holistic approach to design and validation, highlighting the need for collaboration between hardware and software engineers to overcome the inherent complexities of these advanced systems. Ultimately, this research contributes to the ongoing discourse on optimizing design strategies and improving validation techniques in the evolving field of FPGA-based SoC technology.

KEYWORDS: *FPGA, System-On-Chip, Design Challenges, Validation Techniques, Hardware Integration, Software Compatibility, High-Level Synthesis, Automated Verification, Timing Constraints, Digital Design.*

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